ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

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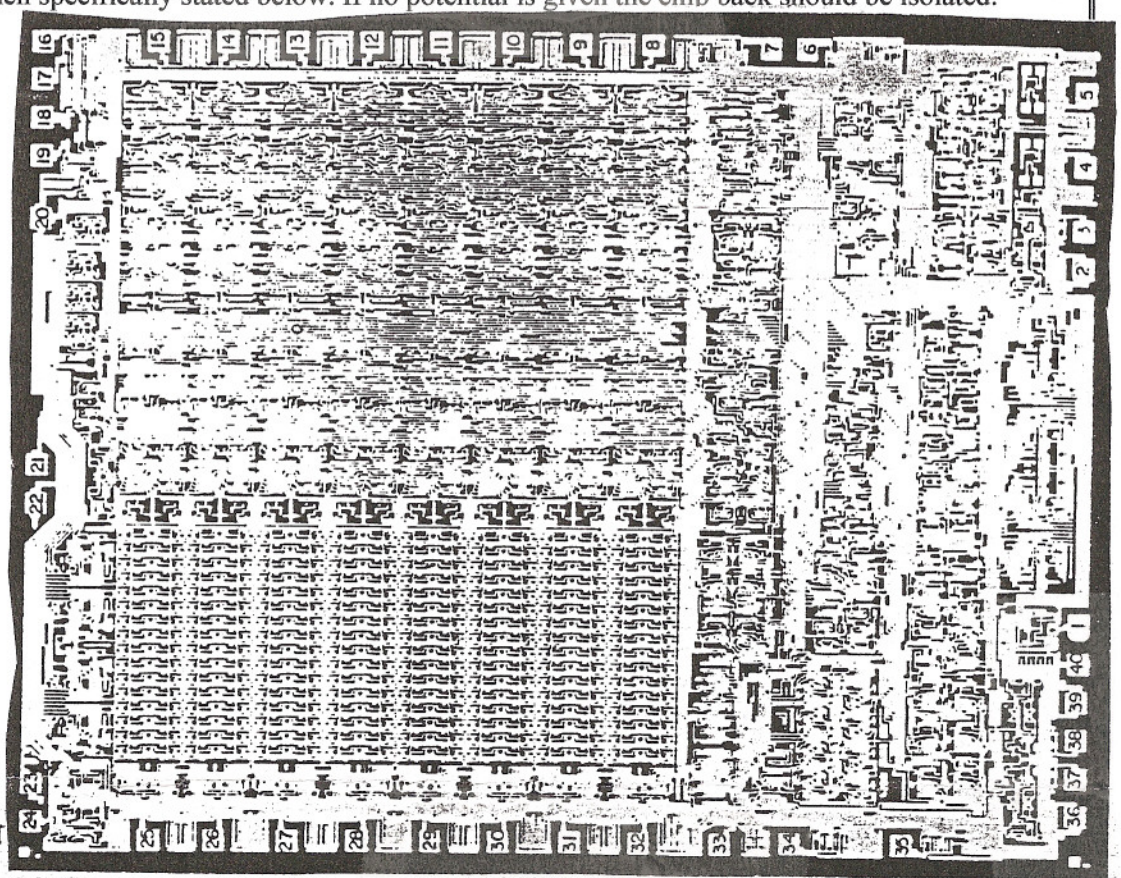
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PIN/PAD	FUNCTION								
1.	CLOCK	9.	BUS 6	17.	N2	25.	MA0	33.	TPB
2.	$\overline{\text{WAIT}}$	10.	BUS 5	18.	N1	26.	MA1	34.	TPA
3.	$\overline{\text{CLEAR}}$	11.	BUS 4	19.	N0	27.	MA2	35.	$\overline{\text{MWR}}$
4.	Q	12.	BUS 3	20.	V_{ss}	28.	MA3	36.	$\overline{\text{INTER-RUPT}}$
5.	SC1	13.	BUS 2	21.	$\overline{\text{EF4}}$	29.	MA4	37.	DMA OUT
6.	SC0	14.	BUS 1	22.	$\overline{\text{EF3}}$	30.	MA5	38.	$\overline{\text{DMA IN}}$
7.	$\overline{\text{MRD}}$	15.	BUS 0	23.	$\overline{\text{EF2}}$	31.	MA6	39.	$\overline{\text{XTAL}}$
8.	BUS 7	16.	V_{cc}	24.	$\overline{\text{EF1}}$	32.	MA7	40.	V_{DD}

APPROVED BY:MG	**DIE SIZE :216X166**	**DATE: 11/17/08**
MFG:RCA	**THICKNESS:**	**P/N:CDP1802AC**